REMARKS

Claims 1 - 36 are pending in this application. Claims 16-34 have been withdrawn from consideration. By this Amendment, claim 1 has been amended to correct a minor informality, and claims 35 and 36 have been added. The applicant respectfully submits that no new matter has been added. It is believed that this Response is fully responsive to the Office Action dated November 23, 1999.

35 U.S.C. §112, Second Paragraph, Rejection:

Claim 1 stands rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

This rejection is respectfully traversed.

Applicant respectfully submits that the amendment to claim 1 obviates the rejection of claim 1 under 35 U.S.C. §112, second paragraph. Accordingly, withdrawal of the rejection of claim 1 under 35 U.S.C. §112, second paragraph, is respectfully solicited.

As to the Merits:

Claims 1-14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over **Uehara et al.** in view of **Hiroshi**.

This rejection is respectfully traversed.

With respect to **Uehara**, the Examiner asserts that **Uehara** discloses in Fig. 6 a semiconductor device having a base 10; two conductor patterns 50b; a protective etch stopper film covering the upper surface of the patterns 18x; a first insulation film 32; a contact hole between the two conductor patterns; sidewall insulation films 20a, 20b; and a plug buried in the contact hole 50a.

However, as discussed in Applicants' previous Amendment of September 2, 1999, **Uehara** does not disclose or fairly suggest the features asserted by the Examiner..

That is, while **Uehara** may disclose in Fig. 6 a contact hole, the region where the withdrawn electrode 31 and the buried layer 33 are formed, and an insulation film 32, **Uehara** does not disclose that the withdrawn electrode 31 is formed in the insulation film 32 by etching the insulation film 32.

Moreover, **Uehara** does not disclose or fairly suggest that the sidewall insulation films (20a,20b) are formed on the inter-layer insulation film 32 in the contact hole. **Uehara** also does not

teach or suggest the insulation film having substantially the same height as the etching stopper film (protecting film 19).

Furthermore, the Examiner asserts that the dummy electrodes 50b of **Uehara** correspond to the conductor patterns of the claims of the present application. However, dummy electrodes 50b are not adjacent to each other since gate electrode 50a is disposed between dummy electrodes 50b.

In addition, the Examiner asserts that the gate electrode 50a corresponds to the plug buried in the contact hole. However, the gate electrode 50a is not the plug, and is not buried in the contact hole.

Moreover, as described in column 15, lines 8-15 of **Uehara**, the sidewall insulation films 20a, 20b are formed on all side walls of the conductor patterns 50a, 50b having protective films 19a, 19b formed thereon. Then, as described in column 15, lines 32-41, the conducting film 31x is deposited and patterned to form the electrodes 31 connected to the source/drain diffusions 21. Thus, in **Uehara**, surface roughness formed by the conductor patterns 50a, 50b is remained before forming the conducting film 31x. Thus, when the conducting film 31x is buried between the conductor patterns 50a and 50b, thickness of the conductor film 31x in the regions between the conductor patterns 50a and 50b is thicker than that in the regions where the conductor pattern 50a, 50b are formed, so that it is difficult to etch the conducting film 31x to form the electrode 31. On the other hand, when the conducting film 31x is not buried between the conductor patterns 50a and 50b, the

photo-resist pattern for patterning the conducting film 31x must be formed on the rough surface, so that it is difficult to form the photo-resist pattern.

These subjects of **Uehara** can be solved by depositing the insulation film and planarizing the surface thereof after forming the sidewall insulation film 20a, 20b and before forming the conducting film 31x. This method is described in Figs. 51A-51D of the present application, which shows the prior art of the present invention. It represents the critical inventive step for introducing to the prior art (Figs. 51A-51D) and the present invention that the contact hole is formed through the insulation film.

Thus, **Uehara** is limited to background prior art of the present invention and is not related to the present claimed invention.

With regard to **Hiroshi**, the Examiner asserts that **Hiroshi** discloses a semiconductor device having an etch stop layer 6 of silicon nitride formed on a gate electrode 5; a first insulating film formed over the etch stopper layer; a contact hole 9 formed in the insulating film between two gate structures and reaching the base substrate; a sidewall insulation film formed on an inner wall of the insulation film, on the side of the gate conductor patterns, and on the side of the etch stopper film.

However, the semiconductor device according to claim 1 has a feature that the sidewall insulation film is formed on an inner wall of the first insulation film, each side wall of the two

conductor patterns, and each side wall of the etching stopper film in the contact hole. As shown in, e.g., Fig. 1 of the present application, the sidewall insulation film 32 is formed on the side walls of the respective gate electrodes exposed in the contact hole. On the other hand, in **Hiroshi**, the sidewall insulation film 12 is only formed on the side wall of one gate electrode 5.

When the sidewall insulation film is formed on the side wall of one gate electrode as described in **Hiroshi**, the contact hole has a smaller size as the disalignment is occur (see page 5, line 18 to page 6, line 6 of the specification of the present application). On the other hand, when the sidewall insulation film is formed on the side wall of the respective gate electrodes exposed in the contact hole, the size of the contact hole does not change even when the disalignment takes place in the lithography step for opening the contact hole (see First Embodiment of the present application).

Hiroshi neither teaches nor suggests the fluctuation of the size of the contact hole by the disalignment and the sidewall insulation film formed on the side walls of the respective gate electrodes.

Thus, **Hiroshi** is clearly different from the present invention and does not provide any motivation for the present invention, so that the present invention would not have been unobvious

to one of ordinary skill in the art at the time the invention was made, based on **Uehara** and **Hiroshi**, singly or in combination.

Thus, it is respectfully asserted that the prior art fails to teach or suggest recitations of claims 1 - 14 and 35 - 36 requested that the Examiner allow these claims, along with the entire application, to issue. Accordingly, withdrawal of the rejection of claims 1 - 14 and 35 - 36 under 35 U.S.C. §103(a) is respectfully solicited.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,

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